SONY

Tentative Ver.0.1 IMX928-AMB

Diagonal 31.9 mm (Type 2.0) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

Description

The IMX928-AMB is a diagonal 31.9 mm (Type 2.0) CMOS active pixel type solid-state image sensor with a square pixel array and 68 M effective pixels. This chip features a global shutter with variable charge-integration time. This sensor operates with 3.3 V, 2.9 V, 1.1 V, and 1.8 V quadruple power supply. High sensitivity and low dark current characteristics are achieved.
(Applications: FA cameras, 3D vision cameras)

Features

◆CMOS active pixel type dots

◆Built-in timing adjustment circuit, H/V driver and serial communication circuit

◆Global shutter function

◆Input clock frequency 37.125 MHz / 74.25 MHz

◆Readout mode

All-pixel scan mode, 1/2 subsampling mode

H2V2 FD binning mode / H1V2 FD binning mode / H2V1 FD binning mode

ROI mode, Vertical / Horizontal - Normal / Inverted readout mode

◆Readout rate (*) At high frame rates, control so as not to exceed Tj = +85 °C

Maximum frame rate in All-pixel scan mode: *controller mode

8-bit 138.9 frames/s,10-bit 126.8 frame/s, 12-bit 90.6 frame/s

◆Variable-shutter speed

◆Pulse Output Function

The monitor output for Integration period (TOUT0) and for internal AD period (TOUT1)

◆8-bit /10-bit / 12-bit Output

◆CDS / PGC function

0 dB to 24 dB: Variable analog Gain (0.3 dB step)* 12-bit

24.3 dB to 48 dB: Fixed analog Gain: 24 dB + variable digital Gain: 0.3 dB to 24 dB (0.3 dB step)*12-bit

0 dB to 18 dB: Variable analog Gain (0.3 dB step)* 8-bit / 10-bit

18.3 dB to 42 dB: Fixed analog Gain: 18 dB + variable digital Gain: 0.3 dB to 24 dB (0.3 dB step)*8-bit / 10-bit

◆I/O interface

SLVS-EC (2 Lane , 4 Lane , 6 Lane , 8 Lane , 4 Lane × 2 , 6 Lane × 2 , 8 Lane × 2) output

SLVS-EC Baud Rate: 4.752 Gbps / lane 9.504 Gbps / lane 12.474 Gbps / lane (Grade 3, 4 and 5)

◆CRA characteristics: The target CRA is 6 degrees at 100% image height.

◆Ceramic package with connector. The connector is floating type.

◆Seal glass: both sides are processed by AR coating

Device Structure

◆CMOS image sensor		
◆Image size	Diagonal 31.9 mm (Type 2.0)	Approx. 68.55 M pixels
◆Total number of pixels	8280 (H) × 8376 (V)	Approx. 69.35 M pixels
◆Number of effective pixels	8280 (H) × 8280 (V)	Approx. 68.55 M pixels
◆Number of active pixels	8256 (H) × 8256 (V)	Approx. 68.16 M pixels
◆Number of recommended recording pixels	8248 (H) × 8248 (V)	Approx. 68.02 M pixels
◆Unit cell size	2.74 µm (H) × 2.74 µm (V)	
◆Optical black	Horizontal (H) direction: Front 0 pixel, rear 0 pixel	
	Vertical (V) direction: Front 20 pixels, rear 0 pixel	
◆Package	Ceramic package with connector	
	160 pin × 2	45 mm (H) × 52 mm (V)

Basic Drive Mode

Drive mode	Recommended number of recording pixels	Maximum frame rate [frame/s]	Output interface	Output [bit]
All-pixel (Controller mode)	8248 (H) × 8248 (V) Approx. 68.02 M pixels	138.9	SLVS-EC 8 × 2 Lane	8
		126.8		10
		90.6		12
H2V2 FD binning 1/2 subsampling	4124 (H) × 4124 (V) Approx. 17.00 M pixels	271.4	SLVS-EC 8 × 2 Lane	8
		248.3		10
		178.3		12

Note: All frame rates are tentative.

Pregius S

* Pregius S and its logo are registered trademarks or trademarks of Sony Group Corporation or its affiliates. Pregius S is a global shutter sensor technology for active pixel-type CMOS image sensors. By stacking the signal processing on the back illuminated type CMOS Image Sensor it realizes small chip size and high sensitivity, whilst using the high picture quality global shutter pixel technology of Pregius.

Image Sensors for Industrial Applications
https://info.sony-semicon.com/en/industry